Claims

1. A synchronizing signal processing circuit for producing, from a first synchronizing signal entering thereto, a second synchronizing signal to be output therefrom, the synchronizing signal processing circuit comprising:

a first counter counting a clock of a predetermined frequency and being reset each time an entry of the first synchronizing signal is detected;

a first gate signal producing circuit for producing a first gate signal which changes to an open state when a count value of the first counter reaches a first value, and changes to a closed state when the first counter is reset and when the count value of the first counter reaches a second value larger than the first value;

a second counter counting the clock and being reset upon each reception of a reset signal;

a self-running synchronizing pulse producing circuit for producing a self-running synchronizing pulse when a count value of the second counter reaches the second value;

a second gate signal producing circuit for producing a second gate signal which changes to the open state when the count value of the second counter reaches the first value, and changes to the closed state when the second counter is reset;

a first gate circuit allowing the first synchronizing signal to pass when at least one of the first and the second gate signals indicates the open state, and blocking the first synchronizing signal at other times;

a synchronizing pulse producing circuit for producing a synchronizing pulse to be output as the second synchronizing signal upon reception of the first synchronizing signal from the first gate circuit and upon reception of the self-running

synchronizing pulse from the self-running synchronizing pulse producing circuit; and

a reset signal producing circuit outputting the reset signal to the second counter upon reception of the first synchronizing signal from the first gate circuit and upon reception of the self-running synchronizing pulse from the self-running synchronizing pulse producing circuit.

2. A synchronizing signal processing circuit according to claim 1, further comprising a mode determination circuit which sets a self-running mode flag when the count value of the second counter reaches the second value and clears the self-running mode flag when the first synchronizing signal passes through the first gate circuit;

the self-running synchronizing pulse producing circuit producing the self-running synchronizing pulse when the count value of the second counter reaches the second value if the self-running mode flag is cleared, and when the count value of the second counter reaches a third value larger than the first value and smaller than the second value if the self-running mode flag is set;

the second gate signal produced by the second gate signal producing circuit changing to the open state when the count value of the second counter reaches the first value if the self-running mode flag is cleared, and when the count value of the second counter reaches a fourth value smaller than the first value if the self-running mode flag is set.

3. A synchronizing signal processing circuit according to claim 2, further comprising a selection signal producing circuit for producing a selection signal which is set when an entry of the first synchronizing signal is detected if the self-running mode flag is cleared and the first gate signal

indicates the closed state, and reset when the count value of the second counter reaches the third value if the self-running mode flag is set and when the first synchronizing signal passes through the first gate circuit irrespective of a state of the self-running mode flag;

the synchronizing pulse producing circuit producing a synchronizing pulse to be output as the second synchronizing signal upon reception of the first synchronizing signal from the second gate circuit and upon reception of the self-running synchronizing pulse from the self-running synchronizing pulse producing circuit if the selection is reset, while outputting the first synchronizing signal that has passed the first gate circuit as the second synchronizing signal if the selection signal is set.

4. A synchronizing signal processing circuit according to claim 2, further comprising a period detecting circuit for detecting a period of the first synchronizing signal, and a device for determining the first to fourth values on the basis of a value of the period detected by the period detecting circuit.

5. A synchronizing signal processing circuit according to claim 1, in which the first synchronizing signal is a vertical synchronizing signal, and the first and the second counters are supplied with a horizontal synchronizing signal as the clock.

6. A synchronizing signal processing circuit for producing, from a first synchronizing signal entering thereto, a second synchronizing signal to be output therefrom, the synchronizing signal processing circuit comprising:

a first counter counting a clock of a predetermined

frequency and being reset each time an entry of the first synchronizing signal is detected;

a first gate signal producing circuit for producing a first gate signal which changes to an open state when a count value of the first counter reaches a first value, and changes to a closed state when the first counter is reset and when the count value of the first counter reaches a second value larger than the first value;

a second counter counting the clock and being reset upon each reception of a reset signal;

a self-running synchronizing pulse producing circuit for producing a self-running synchronizing pulse when a count value of the second counter reaches the second value;

a second gate signal producing circuit for producing a second gate signal which changes to the open state when the count value of the second counter reaches the first value, and changes to the closed state when the second counter is reset;

a first gate circuit allowing the first synchronizing signal to pass when at least one of the first and the second gate signals indicates the open state, and blocking the first synchronizing signal at other times;

a second gate circuit allowing the first synchronizing signal to pass when the second gate signal indicates the open state, and blocking the first synchronizing signal at other times;

a synchronizing pulse producing circuit for producing a synchronizing pulse to be output as the second synchronizing signal upon reception of the first synchronizing signal from the second gate circuit and upon reception of the self-running synchronizing pulse from the self-running synchronizing pulse producing circuit;

a reset signal producing circuit outputting the reset

signal to the second counter upon reception of the first synchronizing signal from the first gate circuit and upon reception of the self-running synchronizing pulse from the self-running synchronizing pulse producing circuit.

7. A synchronizing signal processing circuit according to claim 6, further comprising a mode determination circuit which sets a self-running mode flag when the count value of the second counter reaches the second value and clears the self-running mode flag when the first synchronizing signal passes through the first gate circuit;

the self-running synchronizing pulse producing circuit producing the self-running synchronizing pulse when the count value of the second counter reaches the second value if the self-running mode flag is cleared, and when the count value of the second counter reaches a third value larger than the first value and smaller than the second value if the self-running mode flag is set;

the second gate signal produced by the second gate signal producing circuit changing to the open state when the count value of the second counter reaches the first value if the self-running mode flag is cleared, and when the count value of the second counter reaches a fourth value smaller than the first value if the self-running mode flag is set.

8. A synchronizing signal processing circuit according to claim 7, further comprising a selection signal producing circuit for producing a selection signal which is set when an entry of the first synchronizing signal is detected if the self-running mode flag is cleared and the first gate signal indicates the closed state, and reset when the count value of the second counter reaches the third value if the self-running mode flag is set and when the first synchronizing

signal passes through the first gate circuit irrespective of a state of the self-running mode flag;

the synchronizing pulse producing circuit producing a synchronizing pulse to be output as the second synchronizing signal upon reception of the first synchronizing signal from the second gate circuit and upon reception of the self-running synchronizing pulse from the self-running synchronizing pulse producing circuit if the selection is reset, while outputting the first synchronizing signal that has passed the first gate circuit as the second synchronizing signal if the selection signal is set.

9. A synchronizing signal processing circuit according to claim 7, further comprising a period detecting circuit for detecting a period of the first synchronizing signal, and a device for determining the first to fourth values on the basis of a value of the period detected by the period detecting circuit.

10. A synchronizing signal processing circuit according to claim 6, in which the first synchronizing signal is a vertical synchronizing signal, and the first and the second counters are supplied with a horizontal synchronizing signal as the clock.